WHAT IS CLAIMED IS:

1. A method for efficient access to multiple lines of image data using a memory device with at least one memory module, wherein each memory module has at least one bank with multiple rows, the method comprising the steps of:

maintaining address information of a current row for each bank within each memory module;

receiving a request for an incoming row; and

determining if the incoming row matches the current row based on the address information and if so, immediately accessing the current row without closing and reopening the current row.

2. The method according to Claim 1 wherein the step of maintaining address information comprises the steps of:

setting an open bit when the current row is opened; and

clearing the open bit when the current row is closed.

3. The method according to Claim 1 further comprising the step of maintaining programmable counters to monitor timing parameters and detect legal and illegal actions.

4. The method according to Claim 1 further comprising the step of positioning adjacent lines of the image data in separate memory banks to optimize access to multiple

lines of the image data.

5. The method according to Claim 1 further comprising the step of:

receiving a request for a desired memory format from an external structure; and

selecting the desired memory format from different address multiplexing schemes.

6. The method according to Claim 1 wherein the memory modules are SDRAM modules, each having four banks.

7. A memory controller for efficient access to multiple lines of image data using at least one memory module, wherein each memory module has at least one bank with multiple rows, the memory controller comprising:

means for maintaining address information of a current row for each bank within each memory module;

means for receiving a request for an incoming row; and

means for determining if the incoming row matches the current row based on the address information and if so, immediately accessing the current row without closing and reopening the current row.

8. The memory controller according to Claim 7 wherein the means for maintaining address information comprises:

means for setting an open bit when the current row is opened; and

means for clearing the open bit when the current row is closed.

9. The memory controller according to Claim 7 further comprising programmable counters maintained to monitor timing parameters and detect legal and illegal actions.

10. The memory controller according to Claim 7 wherein adjacent lines of the image data are positioned in separate memory banks to optimize access to multiple lines of the image data.

11. The memory controller according to Claim 7 further comprising:

means for receiving a request for a desired memory format from an external structure; and

means for selecting the desired memory format from different address multiplexing schemes.

12. The memory controller according to Claim 7 wherein the memory modules are SDRAM modules, each having four banks.